KINTEX UltraScale

Core Board
ACKU040
User Manual

Version Record

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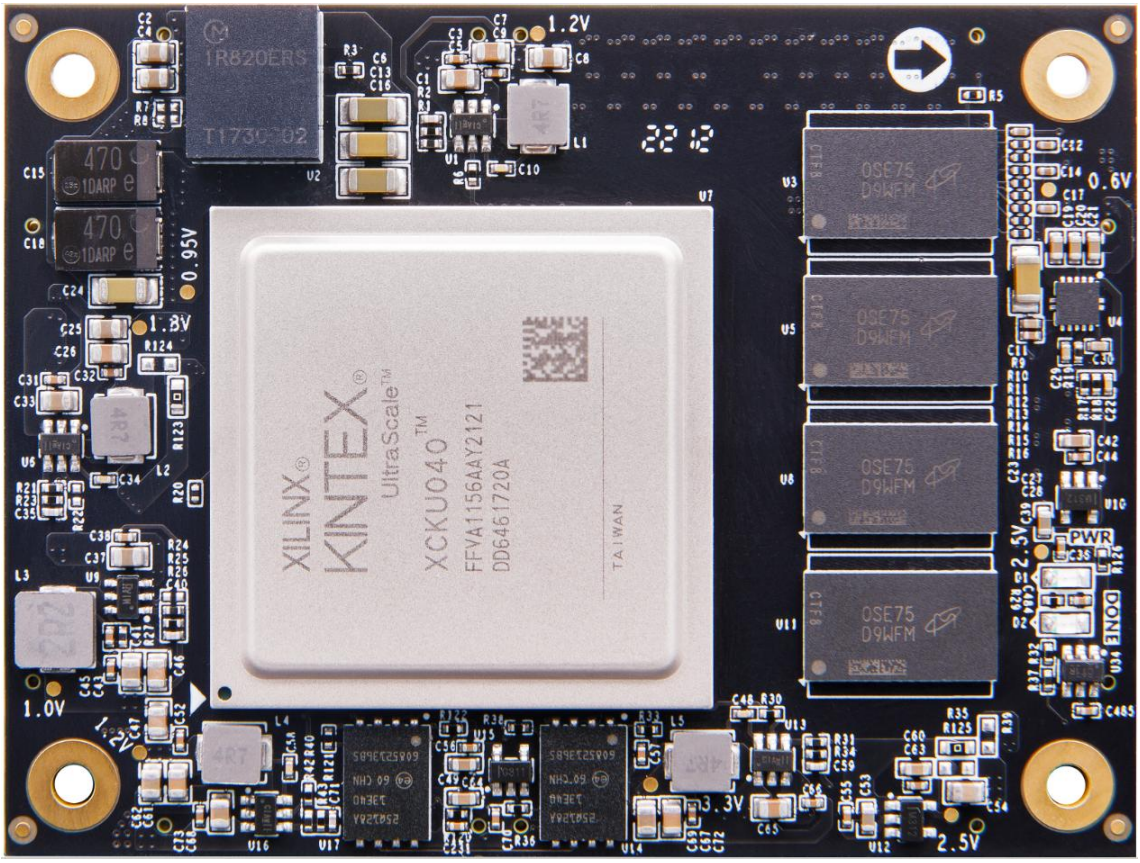
PART 1: ACKU040 Core Board Introduction

ACKU040(core board model,the same below)core board，FPGA chip is based on XCKU040-2FFVA1156I of XILINX company XC7K325 series. The core board used 4 Micron 1GB DDR4 chips MT40A512M16LY-062EIT, with a total capacity of 4GB. In addition, a 128MBit QSPI FLASH is also integrated on the core board,which is used to start storage configuration and system files.

The 4 board-to-board connectors of this core board extend 359 IOs, Of which 104 IO levels of BANK64 and BANK65 is 3.3V, while other IOs levels of BANK is 1.8V; In addition,the core board also extended 20 pairs of high-speed Transceiver GTX interfaces. For users who need a lot of IO, this core board will be a good choice. And IO connection part, the FPGA chip to the interface between the equal length and differential processing, and the core board size is only 80 * 60 (mm), very suitable for secondary development.



ACKU040 Top View

PART 2: FPGA Chip

As mentioned above, the FPGA model we use is XCKU040-2FFVA1156I of XILINX company XC7K325 series. The speed grade is 2,and the temperature grade is industry grade. This model is a FFVA1156 package with 1156 pins, pin pitch is 1.0 mm. Xilinx KINTEX UltraSacale FPGA chip naming rules as below in Figure 1-2-1:

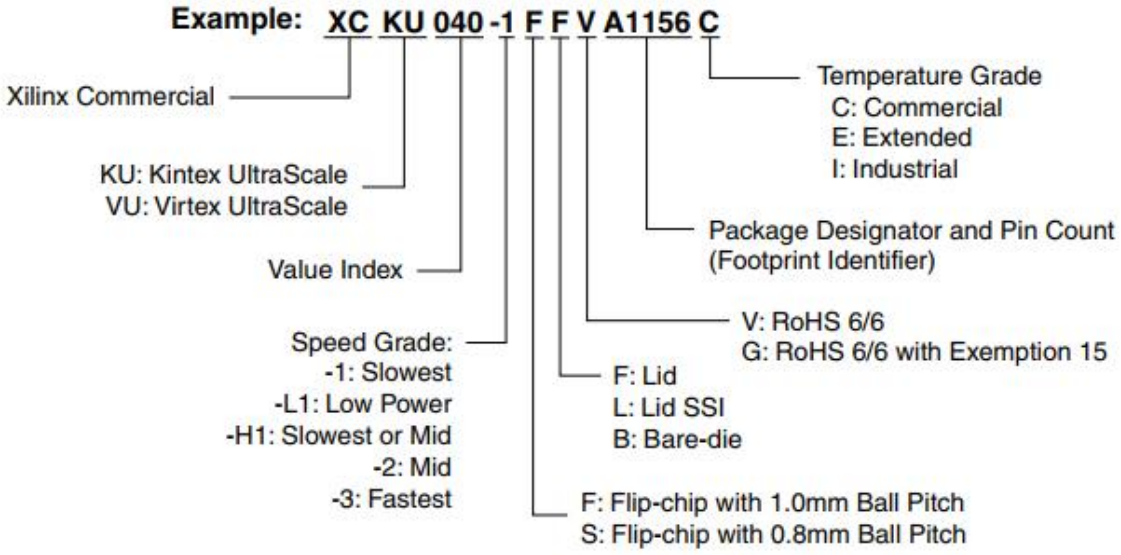


Figure 1-2-1 Definition of Xilinx's KINTEX UltraSacale FPGA series

The main parameters of ACKU040 are as follows:

Name	Specific parameters
Logic Cells	530,250
CLB LUTs	242,400
CLB flip-flops	484,800
Block RAM（Mb)	21.1
DSP Slices	1,920
PCIe Gen3 x8	3
GTH Transceiver	20 个，16.3Gb/s max
Speed Grade	-2
Temperature Grade	Industrial

PART 3: DDR4 DRAM

The FPGA core board ACKU040 equipped with four Micron 1GB DDR4 chips, model MT40A512M16LY-062EIT. Four DDR4 DRAMs make up a 64-bit bus width. Because 4 DDR4 chips are connected to the FPGA, the maximum operating speed of DDR4 SDRAM can reach 1200MHz, Four DDR4 memory systems are directly connected to the BANK44 and BANK46 interfaces of the FPGA. The specific configuration of DDR4 SDRAM is shown in Table 3-1 below.

Table 3-1 DDR4 SDRAM Configuration

Bit Number	Chip Model	Capacity	Factory
U45,U47,U48,U49	MT40A512M16LY-062EIT	512M x 16bit	Micron

The hardware design of DDR4 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR4.

The hardware connection mode of FPGA and DDR4 DRAM is shown in Figure 1-3-1:

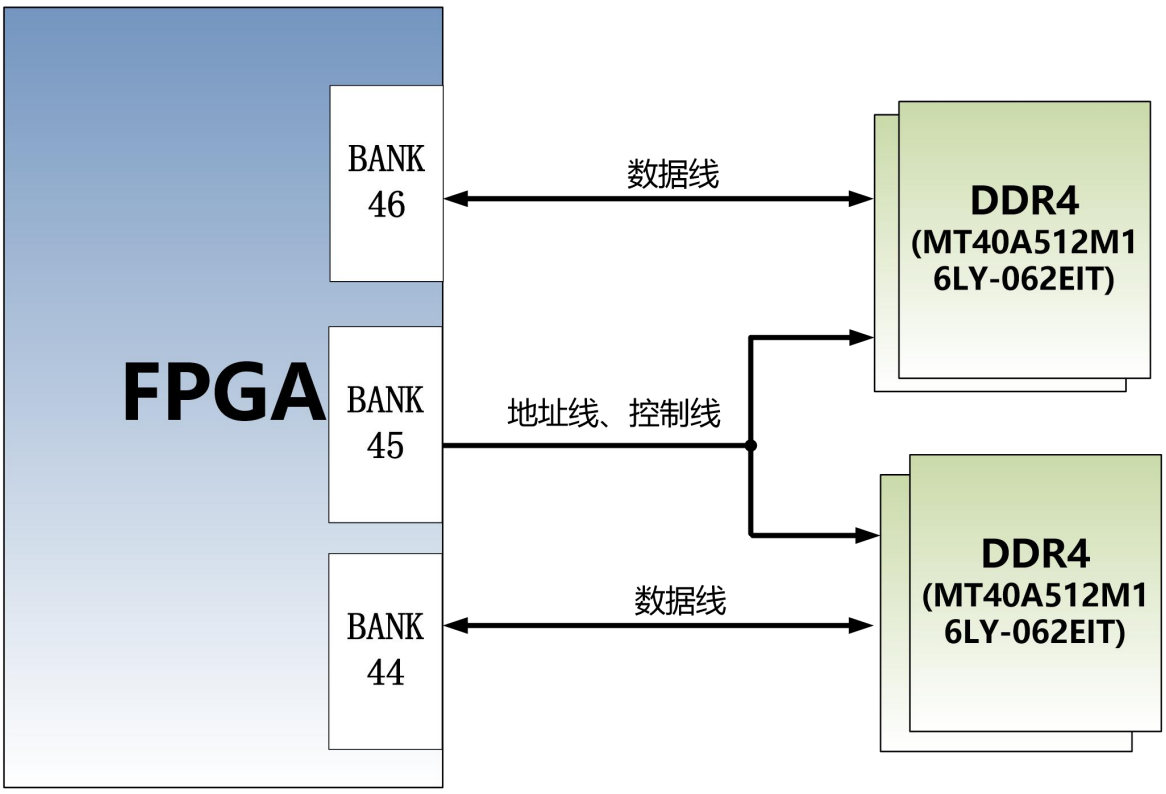


Figure 1-3-1 DDR4 DRAM Schematic

4 DDR4 DRAM pin assignment:

Signal Name	FPGAPIN Name	FPGA P/N
PL_DDR4_DQ0	IO_L3N_T0L_N5_AD15N_44	AE20
PL_DDR4_DQ1	IO_L2N_T0L_N3_44	AG20
PL_DDR4_DQ2	IO_L2P_T0L_N2_44	AF20
PL_DDR4_DQ3	IO_L5P_T0U_N8_AD14P_44	AE22
PL_DDR4_DQ4	IO_L3P_T0L_N4_AD15P_44	AD20
PL_DDR4_DQ5	IO_L6N_T0U_N11_AD6N_44	AG22
PL_DDR4_DQ6	IO_L6P_T0U_N10_AD6P_44	AF22
PL_DDR4_DQ7	IO_L5N_T0U_N9_AD14N_44	AE23
PL_DDR4_DQ8	IO_L8N_T1L_N3_AD5N_44	AF24
PL_DDR4_DQ9	IO_L11P_T1U_N8_GC_44	AJ23
PL_DDR4_DQ10	IO_L8P_T1L_N2_AD5P_44	AF23
PL_DDR4_DQ11	IO_L12N_T1U_N11_GC_44	AH23
PL_DDR4_DQ12	IO_L9N_T1L_N5_AD12N_44	AG25
PL_DDR4_DQ13	IO_L11N_T1U_N9_GC_44	AJ24
PL_DDR4_DQ14	IO_L9P_T1L_N4_AD12P_44	AG24
PL_DDR4_DQ15	IO_L12P_T1U_N10_GC_44	AH22
PL_DDR4_DQ16	IO_L14P_T2L_N2_GC_44	AK22
PL_DDR4_DQ17	IO_L17P_T2U_N8_AD10P_44	AL22
PL_DDR4_DQ18	IO_L15N_T2L_N5_AD11N_44	AM20
PL_DDR4_DQ19	IO_L17N_T2U_N9_AD10N_44	AL23
PL_DDR4_DQ20	IO_L14N_T2L_N3_GC_44	AK23
PL_DDR4_DQ21	IO_L18N_T2U_N11_AD2N_44	AL25
PL_DDR4_DQ22	IO_L15P_T2L_N4_AD11P_44	AL20
PL_DDR4_DQ23	IO_L18P_T2U_N10_AD2P_44	AL24
PL_DDR4_DQ24	IO_L20P_T3L_N2_AD1P_44	AM22
PL_DDR4_DQ25	IO_L23P_T3U_N8_44	AP24
PL_DDR4_DQ26	IO_L20N_T3L_N3_AD1N_44	AN22
PL_DDR4_DQ27	IO_L21N_T3L_N5_AD8N_44	AN24
PL_DDR4_DQ28	IO_L24P_T3U_N10_44	AN23
PL_DDR4_DQ29	IO_L23N_T3U_N9_44	AP25
PL_DDR4_DQ30	IO_L24N_T3U_N11_44	AP23
PL_DDR4_DQ31	IO_L21P_T3L_N4_AD8P_44	AM24

PL_DDR4_DQ32	IO_L2P_T0L_N2_46	AM26
PL_DDR4_DQ33	IO_L6P_T0U_N10_AD6P_46	AJ28
PL_DDR4_DQ34	IO_L2N_T0L_N3_46	AM27
PL_DDR4_DQ35	IO_L6N_T0U_N11_AD6N_46	AK28
PL_DDR4_DQ36	IO_L5P_T0U_N8_AD14P_46	AH27
PL_DDR4_DQ37	IO_L5N_T0U_N9_AD14N_46	AH28
PL_DDR4_DQ38	IO_L3P_T0L_N4_AD15P_46	AK26
PL_DDR4_DQ39	IO_L3N_T0L_N5_AD15N_46	AK27
PL_DDR4_DQ40	IO_L9N_T1L_N5_AD12N_46	AN28
PL_DDR4_DQ41	IO_L12N_T1U_N11_GC_46	AM30
PL_DDR4_DQ42	IO_L8P_T1L_N2_AD5P_46	AP28
PL_DDR4_DQ43	IO_L11N_T1U_N9_GC_46	AM29
PL_DDR4_DQ44	IO_L9P_T1L_N4_AD12P_46	AN27
PL_DDR4_DQ45	IO_L12P_T1U_N10_GC_46	AL30
PL_DDR4_DQ46	IO_L11P_T1U_N8_GC_46	AL29
PL_DDR4_DQ47	IO_L8N_T1L_N3_AD5N_46	AP29
PL_DDR4_DQ48	IO_L14P_T2L_N2_GC_46	AK31
PL_DDR4_DQ49	IO_L18P_T2U_N10_AD2P_46	AH34
PL_DDR4_DQ50	IO_L14N_T2L_N3_GC_46	AK32
PL_DDR4_DQ51	IO_L15N_T2L_N5_AD11N_46	AJ31
PL_DDR4_DQ52	IO_L15P_T2L_N4_AD11P_46	AJ30
PL_DDR4_DQ53	IO_L17P_T2U_N8_AD10P_46	AH31
PL_DDR4_DQ54	IO_L18N_T2U_N11_AD2N_46	AJ34
PL_DDR4_DQ55	IO_L17N_T2U_N9_AD10N_46	AH32
PL_DDR4_DQ56	IO_L21P_T3L_N4_AD8P_46	AN31
PL_DDR4_DQ57	IO_L24P_T3U_N10_46	AL34
PL_DDR4_DQ58	IO_L23N_T3U_N9_46	AN32
PL_DDR4_DQ59	IO_L20P_T3L_N2_AD1P_46	AN33
PL_DDR4_DQ60	IO_L23P_T3U_N8_46	AM32
PL_DDR4_DQ61	IO_L24N_T3U_N11_46	AM34
PL_DDR4_DQ62	IO_L21N_T3L_N5_AD8N_46	AP31
PL_DDR4_DQ63	IO_L20N_T3L_N3_AD1N_46	AP33
PL_DDR4_DM0	IO_L1P_T0L_N0_DBC_44	AD21
PL_DDR4_DM1	IO_L7P_T1L_N0_QBC_AD13P_44	AE25
PL_DDR4_DM2	IO_L13P_T2L_N0_GC_QBC_44	AJ21

PL_DDR4_DM3	IO_L19P_T3L_N0_DBC_AD9P_44	AM21
PL_DDR4_DM4	IO_L1P_T0L_N0_DBC_46	AH26
PL_DDR4_DM5	IO_L7P_T1L_N0_QBC_AD13P_46	AN26
PL_DDR4_DM6	IO_L13P_T2L_N0_GC_QBC_46	AJ29
PL_DDR4_DM7	IO_L19P_T3L_N0_DBC_AD9P_46	AL32
PL_DDR4_DQS0_P	IO_L4P_T0U_N6_DBC_AD7P_44	AG21
PL_DDR4_DQS0_N	IO_L4N_T0U_N7_DBC_AD7N_44	AH21
PL_DDR4_DQS1_P	IO_L10P_T1U_N6_QBC_AD4P_44	AH24
PL_DDR4_DQS1_N	IO_L10N_T1U_N7_QBC_AD4N_44	AJ25
PL_DDR4_DQS2_P	IO_L16P_T2U_N6_QBC_AD3P_44	AJ20
PL_DDR4_DQS2_N	IO_L16N_T2U_N7_QBC_AD3N_44	AK20
PL_DDR4_DQS3_P	IO_L22P_T3U_N6_DBC_AD0P_44	AP20
PL_DDR4_DQS3_N	IO_L22N_T3U_N7_DBC_AD0N_44	AP21
PL_DDR4_DQS4_P	IO_L4P_T0U_N6_DBC_AD7P_46	AL27
PL_DDR4_DQS4_N	IO_L4N_T0U_N7_DBC_AD7N_46	AL28
PL_DDR4_DQS5_P	IO_L10P_T1U_N6_QBC_AD4P_46	AN29
PL_DDR4_DQS5_N	IO_L10N_T1U_N7_QBC_AD4N_46	AP30
PL_DDR4_DQS6_P	IO_L16P_T2U_N6_QBC_AD3P_46	AH33
PL_DDR4_DQS6_N	IO_L16N_T2U_N7_QBC_AD3N_46	AJ33
PL_DDR4_DQS7_P	IO_L22P_T3U_N6_DBC_AD0P_46	AN34
PL_DDR4_DQS7_N	IO_L22N_T3U_N7_DBC_AD0N_46	AP34
PL_DDR4_A0	IO_L18N_T2U_N11_AD2N_45	AG14
PL_DDR4_A1	IO_L23N_T3U_N9_45	AF17
PL_DDR4_A2	IO_L20P_T3L_N2_AD1P_45	AF15
PL_DDR4_A3	IO_L16N_T2U_N7_QBC_AD3N_45	AJ14
PL_DDR4_A4	IO_L19N_T3L_N1_DBC_AD9N_45	AD18
PL_DDR4_A5	IO_L15P_T2L_N4_AD11P_45	AG17
PL_DDR4_A6	IO_L23P_T3U_N8_45	AE17
PL_DDR4_A7	IO_L11N_T1U_N9_GC_45	AK18
PL_DDR4_A8	IO_L24P_T3U_N10_45	AD16
PL_DDR4_A9	IO_L13P_T2L_N0_GC_QBC_45	AH18
PL_DDR4_A10	IO_L19P_T3L_N0_DBC_AD9P_45	AD19
PL_DDR4_A11	IO_L24N_T3U_N11_45	AD15
PL_DDR4_A12	IO_L14P_T2L_N2_GC_45	AH16
PL_DDR4_A13	IO_L10N_T1U_N7_QBC_AD4N_45	AL17

PL_DDR4_BA0	IO_L18P_T2U_N10_AD2P_45	AG15
PL_DDR4_BA1	IO_L10P_T1U_N6_QBC_AD4P_45	AL18
PL_DDR4_BG0	IO_L16P_T2U_N6_QBC_AD3P_45	AJ15
PL_DDR4_WE_B	IO_L9N_T1L_N5_AD12N_45	AL15
PL_DDR4_RAS_B	IO_L8N_T1L_N3_AD5N_45	AM19
PL_DDR4_CAS_B	IO_L8P_T1L_N2_AD5P_45	AL19
PL_DDR4_CKE	IO_L14N_T2L_N3_GC_45	AJ16
PL_DDR4_ACT_B	IO_L21N_T3L_N5_AD8N_45	AF18
PL_DDR4_CLK_N	IO_L22N_T3U_N7_DBC_AD0N_45	AE15
PL_DDR4_CLK_P	IO_L22P_T3U_N6_DBC_AD0P_45	AE16
PL_DDR4_CS_B	IO_L21P_T3L_N4_AD8P_45	AE18
PL_DDR4_OTD	IO_L17P_T2U_N8_AD10P_45	AG19
PL_DDR4_PAR	IO_L20N_T3L_N3_AD1N_45	AF14
PL_DDR4_RST	IO_L15N_T2L_N5_AD11N_45	AG16

PART 4: QSPI Flash

The FPGA core board ACKU040 is equipped with two 128MBit Quad-SPI FLASH, and the model is N25Q128A, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the FPGA configuration Bin files and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 4-1.

Position	Model	Capacity	Factory
U14	N25Q128A	128Mbit	Numonyx

Table 4-1 QSPI FlashQSPI FLASH Specification

QSPI FLASH is connected to the dedicated pins of BANK0 of the FPGA chip. The clock pin is connected to CCLK0 of BANK0,and other data and chip select signals are connected to D00~D03 and FCS pin of BANK0 respectively. Figure 1-4-2 shows the schematic diagram connection of QSPI Flash and FPGA chip.

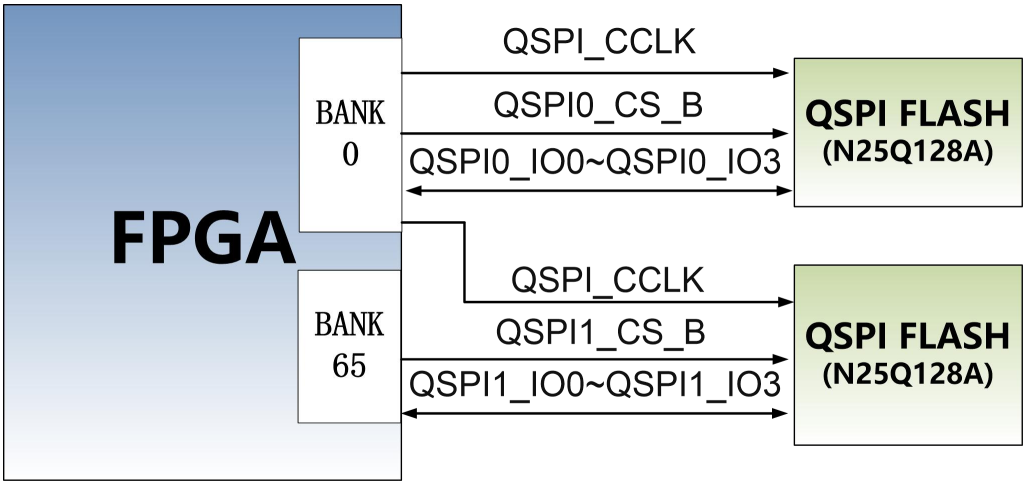


Table 1-4-2 QSPI Flash Schematic diagram

QSPI Flash pin assignments:

Signal Name	FPGA PIN Name	FPGA P/N
QSPI_CCLK	CCLK_0	AA9
QSPI0_CS_B	RDWR_FCS_B_0	U7
QSPI0_IO0	D00_MOSI_0	AC7
QSPI0_IO1	D01_DIN_0	AB7
QSPI0_IO2	D02_0	AA7
QSPI0_IO3	D03_0	Y7

Signal Name	FPGA PIN Name	FPGA P/N
QSPI_CCLK	CCLK_0	AA9
QSPI1_CS_B	IO_L2N_T0L_N3_FWE_FCS2_B_65	G26
QSPI1_IO0	IO_L22P_T3U_N6_DBC_AD0P_D04_65	M20
QSPI1_IO1	IO_L22N_T3U_N7_DBC_AD0N_D05_65	L20
QSPI1_IO2	IO_L21P_T3L_N4_AD8P_D06_65	R21
QSPI1_IO3	IO_L21N_T3L_N5_AD8N_D07_65	R22

PART 5: Clock configuration

200Mhz Active Differential clock

A differential 200MHz clock source is provided on the core board, providing the system clock for the FPGA.The crystal output is connected to the FPGA BANK45, and this clock can be used to drive the DDR controller working clock and other user logic circuits in the FPGA. The schematic diagram of this clock source is shown in Figure

1-5-1.

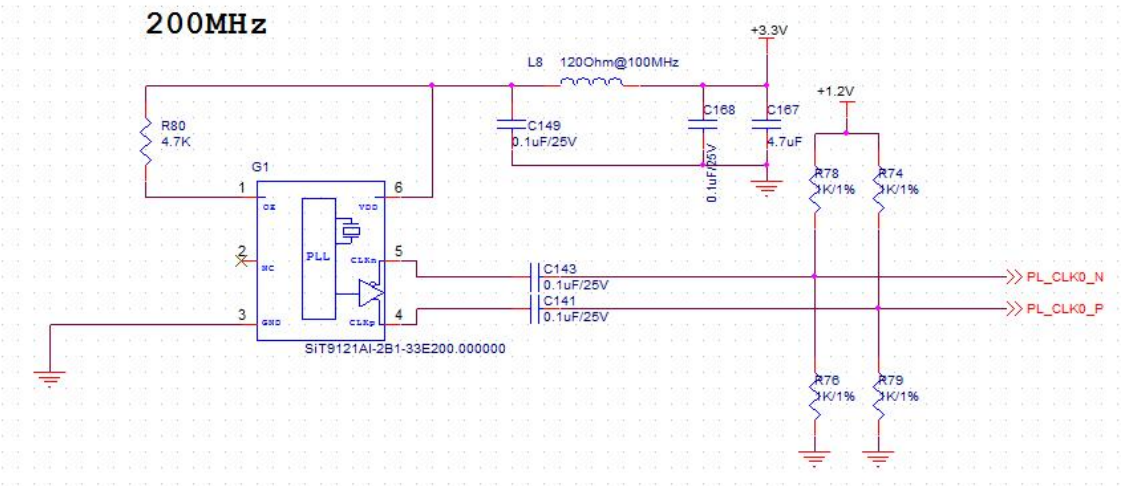


Table 1-5-1

System Reference Clock pin assignments:

Signal Name	FPGA PIN
PL_CLK0_P	AK17
PL_CLK0_N	AK16

PART 6: LED Light

There are 2 red LED lights on the ACKU040 FPGA core board, one of which is power indicator light (PWR),one is the configuration LED light(DONE). When the core board is powered, the power indicator and light (DONE) will illuminate; When the FPGA configuration program, the DONE LED light is off. The schematic diagram of the hardware connection of the LED lamp is shown in Figure 1-6-1:

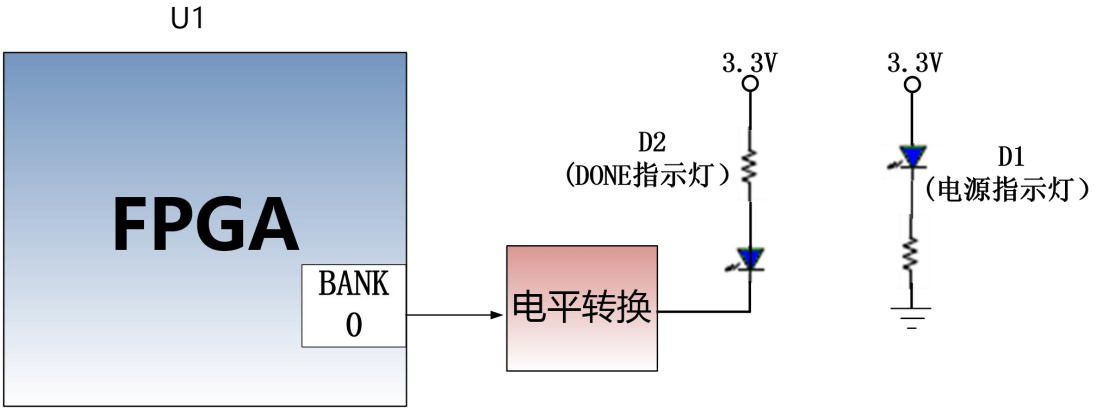


Table1-6-1 LED lights on core board Schematic

PART 7: Power Supply

The power supply voltage of ACKU040 core board is DC12V, which is supplied by connecting the carrier board. The schematic diagram of the power supply design on the core board is shown in Figure 1-7-1 below:

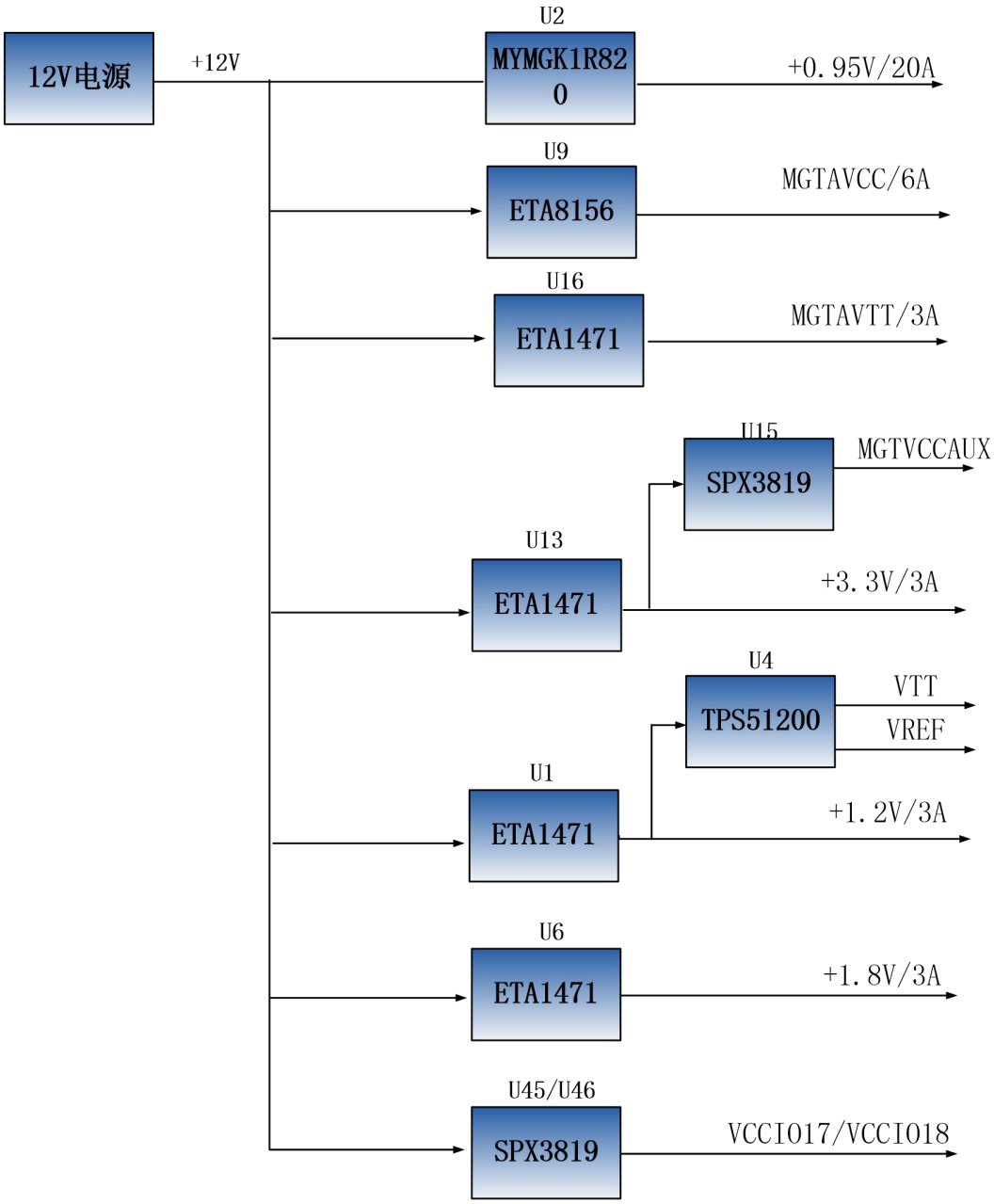


Table 1-7-1Partial Power Interface in Schematic

+12V generates+0.95V FPGA core power through the DCDC power chip MYMGK1R820ERSR. The output current of the MYMGK1R820FRSR is as high as 20A, which far meets the core voltage current demand.The + 12V power is generated by the DCDC chip ETA1471 to generate four power sources: + 1.2V, + 1.8V, +3.3V and

MGTAVTT. The MGTAVCC used by the GTX transceiver is generated by the DCDC chip ETA8156. The GTX auxiliary power + 1.8V through an LDO chip SPX3819-1-8. The VTT and VREF voltages for DDR3 are generated by the TPS51200.

PART 8: Size Dimension

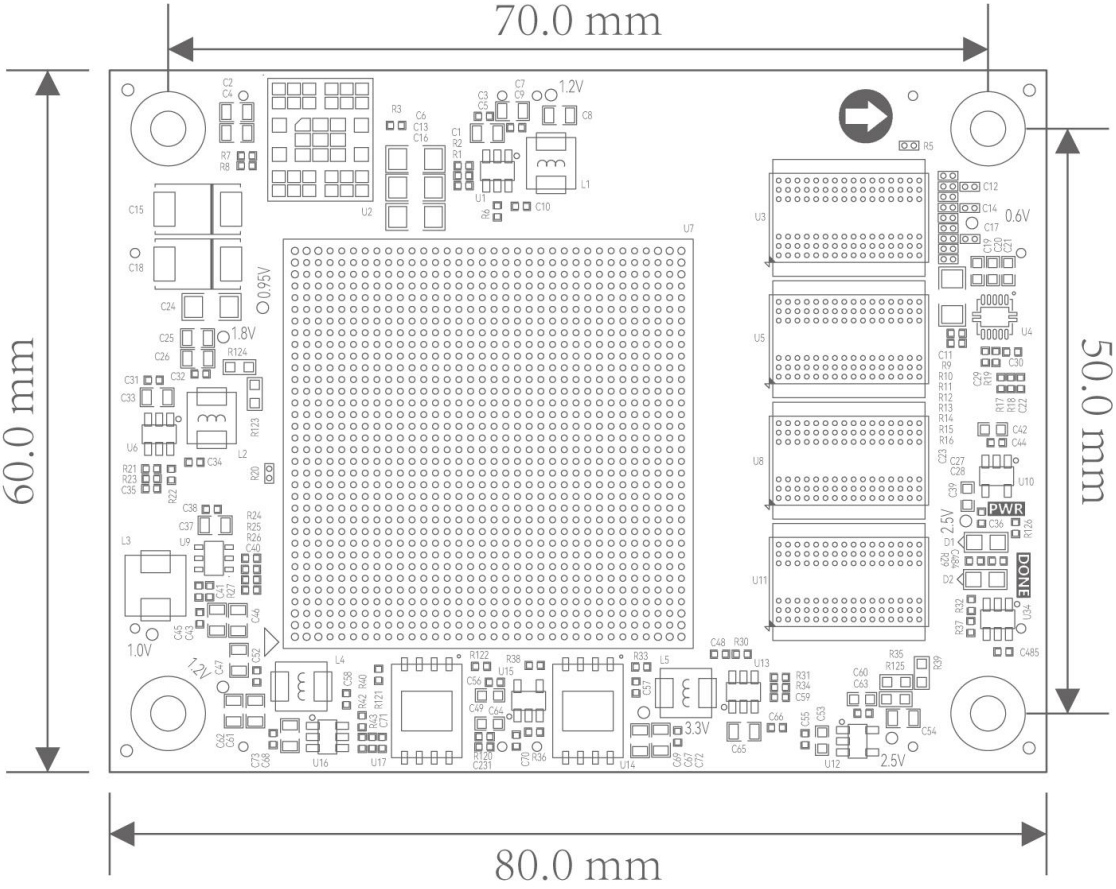


Figure 8-1: (Top View)

PART 9: Board-to-Board Pin Definition

The core board expands a total of six high-speed expansion connectors, and uses four 120-Pin inter-board connectors(J1,J3,J4,J5) and the two 120-Pin inter-board connectors (J2,J6) to connect to the carrier board. The connector uses Panasonic's AXK5A2137YG and AXK580137YG. The connectors of corresponding carrier plates are AXK6A2337YG and AXK680337YG. J1 is connected to the IO of BANK66 and BANK68, J32 is connected to the IO of BANK12 and BANK13 and + 1.8V power.

Pin assignment of J1 connector

J1 Pin	Signal Name	FPGA Pin	J1Pin	Signal Name	FPGA Pin
1	B66_L3_N	C8	2	B66_L1_N	E8
3	B66_L3_P	D8	4	B66_L1_P	F8
5	B66_L7_N	K8	6	B66_L2_N	A9
7	B66_L7_P	L8	8	B66_L2_P	B9
9	GND	-	10	GND	-
11	B66_L9_N	H8	12	B66_L4_N	A10
13	B66_L9_P	J8	14	B66_L4_P	B10
15	B66_L8_N	H9	16	B66_L11_N	F9
17	B66_L8_P	J9	18	B66_L11_P	G9
19	GND	-	20	GND	-
21	B66_L10_N	J10	22	B66_L12_N	F10
23	B66_L10_P	K10	24	B66_L12_P	G10
25	B66_L5_N	C9	26	B66_L6_N	D10
27	B66_L5_P	D9	28	B66_L6_P	E10
29	GND	-	30	GND	-
31	B66_L17_N	K12	32	B66_L13_N	G11
33	B66_L17_P	L12	34	B66_L13_P	H11
35	B66_L19_N	D11	36	B66_L15_N	J11
37	B66_L19_P	E11	38	B66_L15_P	K11
39	GND	-	40	GND	-
41	B66_L16_N	K13	42	B66_L14_N	G12
43	B66_L16_P	L13	44	B66_L14_P	H12
45	B66_L20_N	B12	46	B66_L18_N	H13
47	B66_L20_P	C12	48	B66_L18_P	J13
49	GND	-	50	GND	-
51	B66_L22_N	E13	52	B66_L21_N	B11
53	B66_L22_P	F13	54	B66_L21_P	C11
55	B66_L24_N	C13	56	B66_L23_N	A12
57	B66_L24_P	D13	58	B66_L23_P	A13
59	GND	-	60	GND	-
61	B68_L9_N	F14	62	B68_L19_N	J14
63	B68_L9_P	F15	64	B68_L19_P	J15
65	B68_L8_N	D15	66	B68_L21_N	K15

67	B68_L8_P	E15	68	B68_L21_P	L15
69	GND	-	70	GND	-
71	B68_L15_N	G14	72	B68_L11_N	D16
73	B68_L15_P	G15	74	B68_L11_P	E16
75	B68_L20_N	K17	76	B68_L23_N	J16
77	B68_L20_P	K18	78	B68_L23_P	K16
79	GND	-	80	GND	-
81	B68_L16_N	F19	82	B68_L10_N	D18
83	B68_L16_P	G19	84	B68_L10_P	D19
85	B68_L18_N	H18	86	B68_L1_N	A14
87	B68_L18_P	H19	88	B68_L1_P	B14
89	GND	-	90	GND	-
91	B68_L22_N	J18	92	B68_L3_N	A15
93	B68_L22_P	J19	94	B68_L3_P	B15
95	B68_L24_N	L18	96	B68_L5_N	B16
97	B68_L24_P	L19	98	B68_L5_P	B17
99	GND	-	100	GND	-
101	B68_L13_N	G16	102	B68_L7_N	C14
103	B68_L13_P	G17	104	B68_L7_P	D14
105	B68_L14_N	F17	106	B68_L6_N	C17
107	B68_L14_P	F18	108	B68_L6_P	C18
109	GND	-	110	GND	-
111	B68_L12_N	E17	112	B68_L2_N	A18
113	B68_L12_P	E18	114	B68_L2_P	A19
115	B68_L17_N	H16	116	B68_L4_N	B19
117	B68_L17_P	H17	118	B68_L4_P	C19
119	GND	-	120	GND	-

J2 connector 80 Pin, connect the high speed differential signal of transceiver BANK226~228.

Pin assignment of J2 connector

J2Pin	Signal Name	FPGA Pin	J2Pin	Signal Name	FPGA Pin
1	GND	-	2	GND	-
3	226_TX2_N	U3	4	226_RX2_N	T1
5	226_TX2_P	U4	6	226_RX2_P	T2
7	GND	-	8	GND	-

9	226_TX3_N	R3	10	226_RX3_N	P1
11	226_TX3_P	R4	12	226_RX3_P	P2
13	GND	-	14	GND	-
15	226_CLK1_N	T5	16	226_CLK0_N	V5
17	226_CLK1_P	T6	18	226_CLK0_P	V6
19	GND	-	20	GND	-
21	227_TX0_P	N4	22	227_RX0_P	M2
23	227_TX0_N	N3	24	227_RX0_N	M1
25	GND	-	26	GND	-
27	227_TX1_P	L4	28	227_RX1_P	K2
29	227_TX1_N	L3	30	227_RX1_N	K1
31	GND	-	32	GND	-
33	227_TX2_P	J4	34	227_RX2_P	H2
35	227_TX2_N	J3	36	227_RX2_N	H1
37	GND	-	38	GND	-
39	227_TX3_P	G4	40	227_RX3_P	F2
41	227_TX3_N	G3	42	227_RX3_N	F1
43	GND	-	44	GND	-
45	227_CLK1_P	M6	46	227_CLK0_P	P6
47	227_CLK1_N	M5	48	227_CLK0_N	P5
49	GND	-	50	GND	-
51	228_TX0_P	F6	52	228_RX0_P	E4
53	228_TX0_N	F5	54	228_RX0_N	E3
55	GND	-	56	GND	-
57	228_TX1_P	D6	58	228_RX1_P	D2
59	228_TX1_N	D5	60	228_RX1_N	D1
61	GND	-	62	GND	-
63	228_TX2_P	C4	64	228_RX2_P	B2
65	228_TX2_N	C3	66	228_RX2_N	B1
67	GND	-	68	GND	-
69	228_TX3_P	B6	70	228_RX3_P	A4
71	228_TX3_N	B5	72	228_RX3_N	A3
73	GND	-	74	GND	-
75	228_CLK1_P	H6	76	228_CLK0_P	K6
77	228_CLK1_N	H5	78	228_CLK0_N	K5

79	GND	-	80	GND	-

J3 is the high-speed difference signal of the transceiver BANK224~226 and the partial signal of BANK64, BANK65

Pin assignment of J3 connector

J3 Pin	Signal Name	FPGA Pin	J3 Pin	Signal Name	FPGA Pin
1	B64_L7_N	AF13	2	B64_L21_N	AL9
3	B64_L7_P	AE13	4	B64_L21_P	AK10
5	B64_L11_N	AH12	6	B64_L24_N	AL8
7	B64_L11_P	AG12	8	B64_L24_P	AK8
9	GND	L7	10	GND	-
11	B64_L9_N	AF12	12	B64_L12_N	AH11
13	B64_L9_P	AE12	14	B64_L12_P	AG11
15	B64_L13_N	AG10	16	B64_L14_N	AG9
17	B64_L13_P	AF10	18	B64_L14_P	AF9
19	GND	L7	20	GND	-
21	B64_L10_N	AE11	22	B64_L15_N	AF8
23	B64_L10_P	AD11	24	B64_L15_P	AE8
25	B64_L18_N	AH8	26	B64_L16_N	AE10
27	B64_L18_P	AH9	28	B64_L16_P	AD10
29	GND	L7	30	GND	-
31	B64_L17_N	AD8	32	FPGA_TCK	AC9
33	B64_L17_P	AD9	34	FPGA_TDO	U9
35	B64_L23_N	AJ8	36	FPGA_TMS	W9
37	B64_L23_P	AJ9	38	FPGA_TDI	V9
39	GND	L7	40	GND	-
41	B65_T0U	H23	42	B66_T3U	E12
43	B65_T3U	K22	44	B66_T2U	F12
45	B65_T1U	N23	46	B66_T1U	L9
47	B65_T2U	N27	48	NC	–
49	GND	L7	50	GND	-
51	224_TX0_N	AN3	52	224_RX0_N	AP1
53	224_TX0_P	AN4	54	224_RX0_P	AP2
55	GND	L7	56	GND	-
57	224_TX1_N	AM5	58	224_RX1_N	AM1
59	224_TX1_P	AM6	60	224_RX1_P	AM2

61	GND	L7	62	GND	-
63	224_TX2_N	AL3	64	224_RX2_N	AK1
65	224_TX2_P	AL4	66	224_RX2_P	AK2
67	GND	L7	68	GND	-
69	224_TX3_N	AK5	70	224_RX3_N	AJ3
71	224_TX3_P	AK6	72	224_RX3_P	AJ4
73	GND	L7	74	GND	-
75	224_CLK1_N	AD5	76	224_CLK0_N	AF5
77	224_CLK1_P	AD6	78	224_CLK0_P	AF6
79	GND	L7	80	GND	-
81	225_TX0_N	AH5	82	225_RX0_N	AH1
83	225_TX0_P	AH6	84	225_RX0_P	AH2
85	GND	L7	86	GND	-
87	225_TX1_N	AG3	88	225_RX1_N	AF1
89	225_TX1_P	AG4	90	225_RX1_P	AF2
91	GND	L7	92	GND	-
93	225_TX2_N	AE3	94	225_RX2_N	AD1
95	225_TX2_P	AE4	96	225_RX2_P	AD2
97	GND	L7	98	GND	-
99	225_TX3_N	AC3	100	225_RX3_N	AB1
101	225_TX3_P	AC4	102	225_RX3_P	AB2
103	GND	L7	104	GND	-
105	225_CLK1_N	Y5	106	225_CLK0_N	AB5
107	225_CLK1_P	Y6	108	225_CLK0_P	AB6
109	GND	L7	110	GND	-
111	226_TX0_N	AA3	112	226_RX0_N	Y1
113	226_TX0_P	AA4	114	226_RX0_P	Y2
115	GND	L7	116	GND	-
117	226_TX1_N	W3	118	226_RX1_N	V1
119	226_TX1_P	W4	120	226_RX1_P	V2

J4 connects the signal of BANK48 and the partial signal of BANK64.

Pin assignment of J4 connector

J4 Pin	Signal Name	FPGA Pin	J4 Pin	Signal Name	FPGA Pin
1	B48_L8_N	AG34	2	B48_T2U	AA33
3	B48_L8_P	AF33	4	B48_T1U	AE31
5	B48_L7_N	AG32	6	B48_T3U	V32
7	B48_L7_P	AG31	8	B47_T3U	U29
9	GND	-	10	GND	-
11	B48_L10_N	AF34	12	B48_L18_N	AD33
13	B48_L10_P	AE33	14	B48_L18_P	AC33
15	B48_L9_N	AF32	16	B48_L23_N	V34
17	B48_L9_P	AE32	18	B48_L23_P	U34
19	GND	-	20	GND	-
21	B48_L12_N	AC32	22	B48_L21_N	W34
23	B48_L12_P	AC31	24	B48_L21_P	V33
25	B48_L11_N	AD31	26	B48_L17_N	AB34
27	B48_L11_P	AD30	28	B48_L17_P	AA34
29	GND	-	30	GND	-
31	B48_L13_N	AB32	32	B48_L15_N	AD34
33	B48_L13_P	AA32	34	B48_L15_P	AC34
35	B48_L4_N	AG29	36	B48_L19_N	Y33
37	B48_L4_P	AF29	38	B48_L19_P	W33
39	GND	-	40	GND	-
41	B48_L2_N	AF28	42	B48_L6_N	AG30
43	B48_L2_P	AE28	44	B48_L6_P	AF30
45	B48_L1_N	AF27	46	B48_L5_N	AE30
47	B48_L1_P	AE27	48	B48_L5_P	AD29
49	GND	-	50	GND	-
51	B48_L3_N	AD28	52	B48_L16_N	AB29
53	B48_L3_P	AC28	54	B48_L16_P	AA29
55	B48_L14_N	AB31	56	B48_L24_N	W31
57	B48_L14_P	AB30	58	B48_L24_P	V31
59	GND	-	60	GND	-
61	B48_L20_N	Y30	62	NC	-
63	B48_L20_P	W30	64	NC	-
65	B48_L22_N	Y32	66	NC	-

67	B48_L22_P	Y31	68	NC	-
69	GND	-	70	GND	-
71	B47_T1U	Y22	72	NC	-
73	B47_T2U	Y21	74	NC	-
75	NC	-	76	NC	-
77	NC	-	78	NC	-
79	GND	L7	80	GND	-
81	NC	-	82	NC	-
83	NC	-	84	NC	-
85	NC	-	86	NC	-
87	NC	-	88	POWER_PG	-
89	GND	-	90	GND	-
91	B64_L8_N	AJ13	92	B64_T1U	AJ11
93	B64_L8_P	AH13	94	B64_T3U	AM9
95	B64_L6_N	AL13	96	B64_T0U	AK11
97	B64_L6_P	AK13	98	B64_T2U	AJ10
99	GND	-	100	GND	-
101	B64_L1_N	AP10	102	B64_L2_N	AP13
103	B64_L1_P	AP11	104	B64_L2_P	AN13
105	B64_L4_N	AN12	106	B64_L22_N	AP8
107	B64_L4_P	AM12	108	B64_L22_P	AN8
109	GND	-	110	GND	-
111	B64_L20_N	AP9	112	B64_L19_N	AM10
113	B64_L20_P	AN9	114	B64_L19_P	AL10
115	B64_L3_N	AN11	116	B64_L5_N	AL12
117	B64_L3_P	AM11	118	B64_L5_P	AK12
119	GND	-	120	GND	-

J5 connects the signal of BANK47 and the partial signal of BANK65.

Pin assignment of J5 connector

J5 Pin	Signal Name	FPGA Pin	J5 Pin	Signal Name	FPGA Pin
1	B65_L10_N	K23	2	NC	–
3	B65_L10_P	L22	4	NC	–

5	B65_L6_N	H24	6	B65_L23_N	M21
7	B65_L6_P	J23	8	B65_L23_P	N21
9	GND	L7	10	GND	-
11	B65_L19_N	M22	12	NC	–
13	B65_L19_P	N22	14	B65_L2_P	G25
15	B65_L9_N	K25	16	B65_L1_N	G27
17	B65_L9_P	L25	18	B65_L1_P	H27
19	GND	L7	20	GND	-
21	B65_L24_N	K21	22	B65_L5_N	H26
23	B65_L24_P	K20	24	B65_L5_P	J26
25	B65_L12_N	M24	26	B65_L4_N	J25
27	B65_L12_P	N24	28	B65_L4_P	J24
29	GND	L7	30	GND	-
31	B65_L20_N	P21	32	B65_L3_N	K27
33	B65_L20_P	P20	34	B65_L3_P	K26
35	B65_L7_N	L27	36	B65_L11_N	M26
37	B65_L7_P	M27	38	B65_L11_P	M25
39	GND	L7	40	GND	-
41	B65_L13_N	N26	42	B65_L18_N	P23
43	B65_L13_P	P26	44	B65_L18_P	R23
45	B65_L14_N	P25	46	B65_L15_N	R27
47	B65_L14_P	P24	48	B65_L15_P	T27
49	GND	-	50	GND	-
51	B65_L8_N	L24	52	B65_L17_N	R26
53	B65_L8_P	L23	54	B65_L17_P	R25
55	NC	–	56	B65_L16_N	T25
57	NC	–	58	B65_L16_P	T24
59	GND	L7	60	GND	-
61	B47_L11_N	AA23	62	B47_L19_N	V28
63	B47_L11_P	Y23	64	B47_L19_P	V27
65	B47_L14_N	Y25	66	B47_L22_N	U27
67	B47_L14_P	W25	68	B47_L22_P	U26
69	GND	-	70	GND	-
71	B47_L7_N	AB22	72	B47_L20_N	U25
73	B47_L7_P	AA22	74	B47_L20_P	U24

75	B47_L21_N	Y28	76	B47_L17_N	T23
77	B47_L21_P	W28	78	B47_L17_P	T22
79	GND	-	80	GND	-
81	B47_L3_N	AC24	82	B47_L15_N	U22
83	B47_L3_P	AB24	84	B47_L15_P	U21
85	B47_L23_N	W29	86	B47_L24_N	W26
87	B47_L23_P	V29	88	B47_L24_P	V26
89	GND	-	90	GND	-
91	B47_L10_N	AC21	92	B47_L13_N	W24
93	B47_L10_P	AB21	94	B47_L13_P	W23
95	B47_L5_N	AB27	96	B47_L1_N	Y27
97	B47_L5_P	AA27	98	B47_L1_P	Y26
99	GND	-	100	GND	-
101	B47_L9_N	AB20	102	B47_L12_N	AA25
103	B47_L9_P	AA20	104	B47_L12_P	AA24
105	B47_L4_N	AC27	106	B47_L6_N	AB26
107	B47_L4_P	AC26	108	B47_L6_P	AB25
109	GND	-	110	GND	-
111	B47_L8_N	AC23	112	B47_L16_N	V23
113	B47_L8_P	AC22	114	B47_L16_P	V22
115	B47_L2_N	AD26	116	B47_L18_N	W21
117	B47_L2_P	AD25	118	B47_L18_P	V21
119	GND	-	120	GND	-

J6 connects 12V power, the signal of BANK66 and the partial signal of BANK68.

Pin assignment of J6 connector

J6 Pin	Signal Name	FPGA Pin	J6 Pin	Signal Name	FPGA Pin
1	+12V	-	2	+12V	-
3	+12V	-	4	+12V	-
5	+12V	-	6	+12V	-
7	+12V	-	8	+12V	-
9	+12V	-	10	+12V	-
11	GND	-	12	GND	-
13	B67_L17_N	A20	14	B67_L8_N	A25

15	B67_L17_P	B20	16	B67_L8_P	B25
17	B67_L16_N	C22	18	B67_L6_N	A28
19	B67_L16_P	C21	20	B67_L6_P	A27
21	GND	-	22	GND	-
23	B67_L15_N	B22	24	B67_L13_N	C23
25	B67_L15_P	B21	26	B67_L13_P	D23
27	B67_L11_N	D25	28	B67_L12_N	C24
29	B67_L11_P	E25	30	B67_L12_P	D24
31	GND	-	32	GND	-
33	B67_L18_N	D21	34	B67_L4_N	A29
35	B67_L18_P	D20	36	B67_L4_P	B29
37	B67_L20_N	E21	38	B67_L2_N	B27
39	B67_L20_P	E20	40	B67_L2_P	C27
41	GND	-	42	GND	-
43	B67_L14_N	E23	44	B67_L1_N	E27
45	B67_L14_P	E22	46	B67_L1_P	F27
47	B67_L22_N	F20	48	B67_L10_N	A24
49	B67_L22_P	G20	50	B67_L10_P	B24
51	GND	-	52	GND	-
53	B67_L19_N	F25	54	B67_L9_N	B26
55	B67_L19_P	G24	56	B67_L9_P	C26
57	B67_L24_N	G21	58	B67_L5_N	C28
59	B67_L24_P	H21	60	B67_L5_P	D28
61	GND	-	62	GND	-
63	B67_L21_N	F24	64	B67_L3_N	D29
65	B67_L21_P	F23	66	B67_L3_P	E28
67	B67_L23_N	F22	68	B67_L7_N	D26
69	B67_L23_P	G22	70	B67_L7_P	E26
71	GND	-	72	GND	-
73	B68_T1U	C16	74	B67_T1U	A23
75	B68_T2U	H14	76	B67_T2U	A22
77	B68_T3U	L17	78	B67_T3U	H22
79	NC	–	80	NC	–